

IN THE SPECIFICATION:

Please amend paragraph number [0001] as follows:

[0001] This application is a divisional of application Serial No. 10/347,027, filed January 17, 2003, ~~pending now~~ U.S. Patent 6,744,067, issued June 1, 2004.

Please amend paragraph number [0004] as follows:

[0004] In a typical semiconductor manufacturing process, a multiplicity of integrated circuits is formed as individual dice on a semiconductor wafer. Such a multiplicity of integrated circuits may number in the tens to hundreds, or even thousands (such as in a 300 mm wafer) of individual dice which are generally repeated across the wafer in a two-dimensional array. Once the dice are formed on a semiconductor wafer, the dice are then tested to determine which dice are functional with such a determination performed, generally, by probing each die individually. The probing of individual dice is performed using very costly probe equipment while the die is still in wafer form. Presently available probe equipment contacts each bonding pad on an individual die with a separate probe. A typical probe test requires that each ~~die is~~ die be probed in order to determine the correct and acceptable functionality of each die. However, due to the expensive nature of the probing test equipment, reliability testing (*i.e.*, testing an individual circuit over time) is generally not performed.

Please amend paragraph number [0032] as follows:

[0032] FIG. 3 schematically illustrates ~~wafer 52~~ wafer 51 fabricated in accordance with the preferred patterned interconnection of adjacent dice through the use of patterned conductors which form a portion of the wafer-level test redistribution circuit as described previously with relation to FIG. 1. FIG. 3 illustrates components 50 being coupled to adjacent others of components 50 through the use of patterned conductors 54. To simplify the view of FIG. 3, the bumped contacts 58 of FIG. 2 have not been illustrated in FIG. 3 but are further detailed with reference to FIG. 4. Referring to FIG. 3, patterned conductors 54 gang or otherwise connect in a bus or parallel format a plurality of components 50 for facilitating the conduction of input/output

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